A major purpose of the Technical Information Center is to provide the broadest dissemination possible of information contained in DOE's Research and Development Reports to business, industry, the academic community, and federal, state and local governments.

Although a small portion of this report is not reproducible, it is being made available to expedite the availability of information on the research discussed herein.

1

Los Alamos National Laboratory is operated by the University of California for the United States Department of Energy under contract W-7405-ENG-36

MASTER

LA-UR--86-4286

DE87 003745

TITLE CHARACTERIZATION OF ON-CHIP POLYCRYSTALLINE SILICON PHOTO-CONDUCTORS

AUTHOR(S).

- D. K. Fitzpatrick (Harris emiconductor, Melbourne, FL) /
- D. R. Bowman (U.S. Military Academy, West Point, NY)
- R. B. Hammond (LANL, E-11)

SUBMITTED TO

Proceedings of the International Conference on High-Speed Electronics, August 7-9, 1986, Stockholm, Sweden.

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

By acceptance of this article, the publisher recognizes that the U.S. Government retains a nonexclusive, royally-free license to publish or reproduce the published form of this contribution, or to allow others to do so, for U.S. Government purposes

The Los Alamos National Laboratory requests that the publisher identify this article as work performed under the auspides of the U.S. Department of Energy



LOS Alamos National Laboratory Los Alamos, New Mexico 87545

SILICON PHOTOCONDUCTORS

D. K. Fitzpatrick Harris Semiconductor, Melbourne, FL 32901

D. R. Bowman U. S. Military Academy, West Point, NY 10996

R. B. Hammond Los Alamos National Laboratory, Los Alamos, NM 87545

1. Introduction

Several optoelectronic approaches have been proposed for measuring the high-speed transient response of electronic devices and circuits [1]-[4]. Most of these approaches, however, cannot be used to perform on-chip measurements of silicon integrated circuits because of process incompatibilities. This paper describes measurements and analysis of integrated polycrystalline-silicon photoconductors (PCEs) that have been developed to perform high-speed measurements on silicon substrates.

The development of integrated PCEs for ultrafast electrical pulse generation and sampling on silicon substrates has been previously reported [5]. These PCEs, when stimulated with femtosecond dye laser pulses, can be used for high-frequency characterization of silicon integrated devices, interconnects, and circuits at frequencies up to 100 GHz, and with time resolution as short as one picosecond[5],[6].

Here we report experimental and modeling studies of on-chip photoconductor pulse generation and sampling. Specifically, we discuss a) the effect of ion-beam damage on carrier lifetime and sampling-aperture time, b) the circuit limits to pulse risetime, and c) the room-temperature stability of ion-beam-damaged sampling gates.

2. PCE Fabrication and Measurements

PCEs were fabricated as pulsing and sampling elements in an integrated circuit microstrip transmission-line test structure (see Fig. 1). The transmission line structures consist of 0.8-micron-thick aluminum conductors in 50 and 100 micron widths on both p and n-type silicon substrates. Substrate resistivities vary between 6 and 14 ohm-cm. The PCEs themselves are fabricated in a 0.5 micron undoped polysilicon layer deposited on a field oxide by low-pressure-chemical-vapor-deposition.

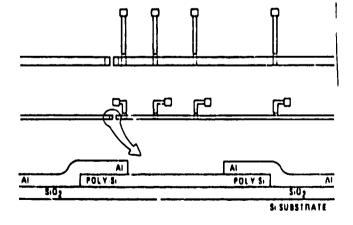


Fig. 1. Schematic diagram of on-chip-photoconductor/ interconnect test structure

A PCE is a rectangular area of polysilicon with metal lines contacting opposite sides of the rectangle. High dark resistance is achieved by using undoped polysilicon. After the polysilicon layer is patterned, the wafer is subjected to a high temperature anneal (1150°C for one hour in an Argon ambient) to increase the average grain size and improve carrier mobilities within the photoconducting region [7],[8]. Aluminum transmission lines are deposited and patterned following this anneal.

To study the effects of ion-beam damage on carrier lifetime and sampling aperture time of the PCEs, the PCE photoconductive regions were irradiated with 250 KeV silicon to doses of 1.5×10^{14} , 3.0×10^{14} , and 5.0×10^{14} cm⁻². Implant doses of these magnitudes are not sufficient to amorphize silicon, but produce a point defect density of approximately 5×10^{22} cm⁻³. Silicon is used as an implant species because it is electrically inert within silicon and has a sufficiently low critical energy (162 KeV), E_c , to be within the capability of common ion implanters. E_c describes the implant energy for a particular species above which the induced damage is primarily the result of nuclear collisions, which cause the most lattice discorder, and hence the fastest carrier relaxation times. Because the amount of damage is only a weak function of the implant energy above E_c , the number of trapping sites (and, thus, the photoconductor recombination rates) can be tailored within a limited range by controlling only the dose for a particular implant species and energy [8].

3. Experimental Results and Data Analysts

The measurement technique utilized in this work is the same as reported in [6],[8]. Here we use the characteristics of the correlation signal to characterize the PCE response. The risetime of the correlation signal is used to determine the effect of the ion damage and circuit environment on the performance of the PCE. All correlation measurements are taken at the second sampler (signal propagation distance = 500 microns, see Fig. 1) in order to avoid local modes near the pulse generator as well as dispersion [9].

The microstrip test structures were fabricated in both 50 and 100 micron widths. These line widths, along with the physical characteristics of the substrate, produced transverse electromagnetic (TEM) impedances of approximately 92 and 76 ohms, respectively. Both structures use a 10-micron gap in the transmission line for the active region of the pulsing photoconductor.

Figure 2 shows the measured risetime of the correlation signal plotted versus transmission-line width. The measured data is prosented with sampler implant dose as a parameter and contains experimental errors estimated to be +/-0.5 picosecond... Prior experimental work [6],[8] has shown an inverse relationship between the dose and recombination rates in the PCE. This is also confirmed by these measurements. In going from a sample dose of 1.5 x 10^{14} cm⁻² Si to a dose of 3 x 10^{14} cm⁻² the risetimes of the correlation signals decrease for both the 50 and 100 micron-wide test structures. If the dosage is increased further to 5 \times 10¹⁴ cm⁻² circuit limits in the 100 micron-wide line mask any decrease in risetime due to shorter carrier lifetime. In contrast, the 50 micron-wide line shows a decrease in risetime for this higher dose. From this observation we conclude that for the 100 micron-wide test structure the optimum dose of 250 keV silicon is between 3 x 10^{14} and 5 x 10^{14} cm⁻². The fastest response possible for the 50 micron-wide structures remains to be determined.

The results of the measurements on the 50 micron-wide line indicate that the structure is not circuit limited while the 100-micron-wide line

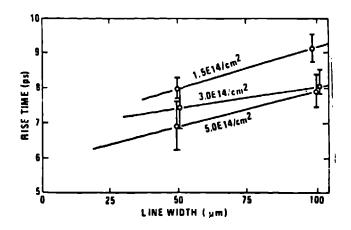


Fig. 2. Plot of correlation risetimes vs line width for 3 implant doses

structure becomes circuit limited at 5 X 10¹⁴ cm⁻². In our previous work, carrier relaxation times within the PCEs limited observed response. Then we approximated PCE response as an initial rising step that decayed exponentially. The rising edge of the correlation signal was due only to carrier relaxation within the sampler. In the circuit-limited case, this assumption is invalid. We must use more rigorous techniques to analyze the data. We accomplish this ty implementing available PCE [10] and microstrip models in an analysis program, MIPCEM (Microstrip and Photoconductive Element Modelling program [8]).

We performed computer simulations of our experiments with MIPCEM to assess the validity of the models and to determine the relaxation times in the sampling gates. In the fits only the recombination rates within the sampler and pulser PCEs were varied. The results of these simulations are summarized in Table I. The simulations agree very well with the data. In all cases, it was possible to extract the recombination parameters of the PCEs from the 50 micron-wide structures and use them to predict the measured response on the 100 micron-wide structures within experimental and model error.

Figure 3 shows a series of measurements taken six months after the data of Fig. 2, plotted in comparison with the initial measurements. The increase in the response time of the PCEs is due to the room temperature annealing of the implant damage over a six month period. The data show a wide variation in response.

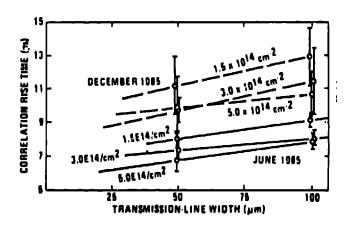


Fig. 3. Same as Fig. 2 except results taken six months after damage implant are also plotted

TABLE I - MEASURED VERSUS SIMULATED CORRELATION RISETIME

| Implant Dosage | <u>Risetime</u> 50-um | <u>Risetime</u> 100-um |
|---------------------------------------|--------------------------|---------------------------|
| | 34 - F III | 200 μ |
| 1.5X10 ¹⁴ cm ⁻² | | |
| Messured | 8.0 ps | 9.3 ps |
| Simulated $(\tau=3.7ps)$ | 7.8 ps | 9.0 ps |
| Relative Error | 3.0 % | 3.2 % |
| 3.0x10 ¹⁴ cm ⁻² | | |
| Measured | 7.3 ps | 8.1 ps |
| Simulated (T=3.0ps) | 6.9 ps | 8.1 ps |
| Relative Error | 6.0 % | 0.0 % |
| 5.0X10 ¹⁴ cm ⁻² | | |
| Measured | 6.7 ps | 7.9 ps |
| Simulated (T=2.8ps) | 6.7 ps | 7.9 ps |
| Relative Error | 0.0 % | 0.0 % |

REFERENCES

- [1] N. S. Nahman, "Picosecond-domain waveform measurements," IEEE Proc., Vol. 66, pp. 441-454, 1978.
- [2] N. S. Nahman "Picosecond-domain waveform measurements," IEEE Trans. Instru. Meas., Vol. IM-32, pp. 177-124, 1983.
- [3] J. K. Everad and J. F. Carrol, "Practical comparison of optoelectronic sampling systems and devices," IEE Proc., Vol. 130, pt. I, pp. 5-16, 1983.
- [4] P. R. Smith, D. H. Auston, A. M. Johnson, and W. M. Augustynaik, "Picosecond photoconductivity in radiation-damaged silicon-on-sapphire films," Appl. Phys. Lett., Vol. 38, pp. 47-50, 1981.
- [5] D. R. Bowman, R. B. Hammond, and R. W. Dutton, "Polycrystallinesilicon integrated photoconductors for picosecond pulsing and gating," IEEE Electron Device Lett., Vol. EDL-6, pp 502-504, 1985.
- [6] D. R. Bowman, R. B. Hammond, and R. W. Dutton, "New integrated polysilicon photoconductor for ultrafast measurements on silicon," Tech. Dig. Int. Electron Devices Mtg., Washington, D.C., December, 1985, pp. 117-120.
- [7] R. B. Hammond and N. M. Johnson, "Impulse photoconductance of thin-film polycrystalline silicon," J. Applied Physics, Vol. 59, pp. 3155-3159, 1986.
- [8] D. R. Bowman, PhD dissertation, Stanford University, Stanford, CA, 1986.
- [9] K. W. Goosen and R. B. Hammond, "Time-domain analyses of picosecond-pulse propagation in microstrip interconnections on si integrated circuits," Manuscript in preparation.
- [10] D. H. Auston, "Impulse response of photoconductors in transmission lines," IEEE J. Quantum Electron., Vol. GE-19, pp. 609-648, 1983.